What is claimed is:

1. A clock divider of a DLL (delay locked loop), comprising:

clock dividing means for receiving a source clock of the DLL to generate a plurality of divided clocks each having a period different from each other;

test mode clock providing means for selectively outputting the plurality of the divided clocks in a test mode in response to a test mode signal and a test mode period selecting signal; and

normal mode clock providing means for outputting selected one of the plurality of the divided clocks in a normal mode in response to the test mode signal.

2. The clock divider of the DLL as recited in claim 1, wherein the test mode clock providing means includes:

decoding means for decoding the test mode period selecting reference signal in response to the test mode signal to output a test mode period selecting signal; and

test mode clock selecting means for outputting one of the plurality of the divided clocks in response to the test mode period selecting signal.

3. The clock divider of the DLL as recited in claim 1, wherein the normal mode clock providing means includes:

normal mode clock option processing means for receiving

the plurality of the divided clocks to output a divided clock that is fixed depending on an option; and

switching means for outputting the fixed divided clock from the normal mode clock option processing means in response to the test mode signal.

4. The clock divider of the DLL as recited in claim 2, wherein the test mode period selecting reference signal is inputted through a predetermined number of address pins in the test mode.

5. The clock divider of the DLL as recited in claim 4, wherein the decoding means includes:

a plurality of NAND gates, each for receiving the test mode signal as its one input and one of combinations of the signals on the address pins and the inverted ones of the signals on the address pins; and

a number of inverters for inverting the output signals of the NAND gates, respectively.

6. The clock divider of the DLL as recited in claim 5, wherein the test mode clock selecting means includes a plurality of transfer gates for outputting the divided clock under control of outputs of the plurality of the inverters, respectively.

7. The clock divider of the DLL as recited in claim 3,

wherein the normal mode clock option processing means includes one of a fuse option, an anti-fuse option and a metal option.

8. The clock divider of the DLL as recited in claim 3, wherein the switching means includes a transfer gate that is controlled by the test mode signal.